Remarks

Claims 1-5 are pending in the application. Claims 1-5 are rejected. The Specification is objected to. Claims 1, 4, and 5 are amended. The Specification is amended. All rejections and objections are respectfully traversed.

The specification is objected to at page 7, line 28. The Specification is amended to overcome the objection.

Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 4 and 5 are amended to overcome the rejections.

Claims 4 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Gallo, et al. (U.S. 6,907,469 – "Gallo").

Regarding independent claims 4 and 5, the invention reduces traffic on an uplink between an edge switch and a core router by performing a layer 3 (Network) address look-up at the edge switch *only if* a packet has a layer 2 destination (MAC) address for the core router. This reduces round trips between the edge switch and the core router across the downlink for packets between devices locally connected to the edge device simply because devices locally connected to the switch may be on a different VLAN, which requires a Network address (Layer 3) look-up. In the prior art, that Layer 3 look-up is done at the router as opposed to the edge switch. According to the invention, the edge switch only performs layer 3 look-ups for packets with MAC destination addresses for the core router. There is no such limitation

described in Gallo.

Gallo describes a single L2/L3 network switch/router including a logical bridge (layer 2), a logical router (layer 3), and one or more control points (CP). Gallo is explicitly directed to handling frames originating from or directed to a control point, see, col. 2, lines 19-20, below:

In view of the above, an improved method of handling [20] frames destined for or originating from the CP is needed.

See also, col. 2, lines 23-33, below:

According to the present invention, the logical bridging [25] function for frames destined for or originating from the CP is offloaded from the CP to a network processor. In a preferred embodiment, frames destined for or originating from the CP are sent to a network processor directly connected to the CP. The network processor performs all the L2 [30] level bridging operations needed by the CP, including MAC address learning for incoming frames, and destination address look-ups and frame forwarding for frames originating from the CP.

The claims as amended distinguish the switch as an L2/L3 capable edge switch, and the router as a core router (generally also L2/L3), which are two distinct devices connected via an uplink. The internal processing of packets within a single L2/L3 bridge/router described in Gallo can therefore never anticipate what is claimed because, as a person of ordinary would readily understand that the invention performs a Layer 3 look-up *only if* the packet has a Layer 2 MAC destination address of the core router, which can result in the beneficial reduction of packet traffic across the uplink if the Layer 3 IP address is for a device locally connected to the edge switch. Otherwise, the packet is sent to the router via the uplink. In contrast, Gallo describes a device that performs L2/L3 bridging and routing according to the prior art and without the conditional look-up for avoiding the uplink recited in the claims. Further, Gallo is directed only to packets that originate from or are destined for a CP within a single device, not packets passing through a switch that are destined for a core router, as claimed. The Examiner is

requested to specifically point out, citing column and line, where Gallo teaches an edge switch performing an L3 network address look-up *only if* the MAC destination address is for a core router connected to the edge switch by an up-link to transmit the packet directly to the destination local to the edge switch instead of the core router via the uplink, as claimed. The combination of logical switch and logical router in a single device as taught by Gallo can never anticipate what is claimed. In short, Gallo performs L3 processing if the MAC destination address of a packet is for the CP of the Gallo device. That is a normal, prior art router function. In contrast, the invention performs an L3 lookup if the MAC destination address of a packet is that of a different L3 device, which is connected to the edge switch by an uplink.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuichi (U.S. 6,363,072) in view of Gallo.

Furuichi is referenced to show operating a network switch which is an edge switch in an Ethernet communication network having a multiplicity of sub-nets. While the applicants agree that Furuichi shows edge switches, route servers and sub-nets, the Applicants do not agree that Furuichi teaches an Ethernet communication network that can use the invention. In fact, an ATM network cannot use the invention because of the *connection-oriented* operation of ATM networks, which map the entire route of an ATM cell prior to transmission from a source device. In contrast, the invention works by leveraging the *connectionless* operation of Ethernet networks, where the source and destinations are known, but the specific route of a packet is determined on the fly by devices between the source and destination devices.
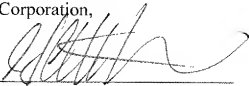
Therefore, while there exist similarities between ATM and Ethernet, the fundamental operation of the invention in changing expected packet paths excludes ATM networks from both the benefit of the invention, and as relevant prior art.

The shortcomings of Gallo have been stated above. Gallo fails to teach an L3 look-up by an edge switch only in response to a MAC address for a core router connected to the edge switch via an uplink, as claimed. Therefore, the rejection should be reconsidered and withdrawn.

It is believed that this application is now in condition for allowance. A notice to this effect is respectfully requested. Should further questions arise concerning this application, the Examiner is invited to call Applicant's attorney at the number listed below. Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account <u>50-3650</u>.

Respectfully submitted,
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